In the Claims:

Please amend claims 1-10 and add new claims 11 and 12 as indicated in the following listing of claims, which replaces all prior versions.

1. (Presently Amended) A switch mode power supply circuit including at least one inductive component coupled to an associated switch ~~switching means~~ for cyclically connecting the inductive component to a source of power, the circuit including a signal output representative of a voltage at a junction of the at least one inductive component to the associated switch ~~switching means~~, the circuit further comprising a hard switching amplitude detector for deriving a measure of hard switching amplitude occurring in operation in the associated switch ~~switching means~~, the detector including a signal processing path for receiving the signal output and generating the measure of hard switching amplitude therefrom, the signal path including:

a signal differentiator circuit ~~differentiating means~~ for imperfectly differentiating the signal output to generate a corresponding imperfectly differentiated signal; and

a signal integrator circuit ~~integrating means~~ for integrating the imperfectly differentiated signal in a temporally-gated manner for generating the measure of hard switching.

2. (Presently Amended) A circuit according to claim 1, wherein the detector further includes a timing circuit ~~means~~ for applying temporal gating to the integrator circuit ~~integrating means~~.

3. (Presently Amended) A circuit according to claim 2, wherein the timing circuit is ~~means are also~~ arranged to provide temporal gating to the differentiator circuit ~~differentiating means~~.

4. (Presently Amended) A circuit according to claim 2, wherein the circuit is ~~means are~~ arranged to reset at least one of the differentiator circuit ~~differentiating means~~ and the integrator circuit ~~integrating means~~ for each conduction cycle of the associated switch

~~switching means~~.

5. (Presently Amended) A circuit according to claim 1, wherein each conduction cycle of the associated switch ~~switching means~~ has associated therewith, in operation:

a downward stroke whereat the associated switch ~~switching means~~ switches from a ~~substantially~~ non-conductive state to a ~~substantially~~ conductive state; and

an upward stroke whereat the associated switch ~~switching means~~ switches from a ~~substantially~~ conductive state to a ~~substantially~~ non-conductive state, the detector being arranged so as to be capable of imperfectly differentiating and subsequently integrating the output signal in a period commencing shortly prior to the upward stroke and ending shortly after completion of the downward stroke of each cycle for deriving the measure of hard switching amplitude during that cycle.

6. (Presently Amended) A circuit according to claim 1, wherein each conduction cycle of the associated switch ~~switching means~~ has associated therewith, in operation:

a downward stroke whereat the associated switch ~~switching means~~ switches from a ~~substantially~~ non-conductive state to a ~~substantially~~ conductive state;

and an upward stroke whereat the associated switch ~~switching means~~ switches from a ~~substantially~~ conductive state to a ~~substantially~~ non-conductive state, the detector being arranged so as to be capable of imperfectly differentiating and subsequently integrating the output signal in a period;

commencing ~~substantially~~ from the end of a first differential signal peak ~~(210)~~ arising from the downward stroke of each cycle to include a subsequent second differential signal peak arising within the cycle after the first peaks; and

ending within or after the second differential signal peak, for deriving the measure of hard switching amplitude during that cycle.

7. (Presently Amended) A circuit according to claim 1, wherein the differentiator circuit is ~~differentiating means are~~ implemented as a potential divider combination of a resistor and an associated capacitor, the resistor and capacitor defining an associated time constant capable of rendering the combination susceptible to providing imperfect

differentiation of the signal output suitable for use in generating the measure of hard switching amplitude.

8. (Presently Amended) A circuit according to claim 1, wherein the differentiator circuit is ~~differentiating means are~~ implemented as a potential divider combination of a resistor and an associated inductor, the resistor and inductor defining an associated time constant capable of rendering the combination susceptible to providing imperfect differentiation of the signal output suitable for use in generating the measure of hard switching amplitude.

9. (Presently Amended) A circuit according to claim 1, the circuit adapted for incorporation ~~being susceptible for use~~ in at least one of: switch mode power supplies, motor controllers, battery chargers, ionizing apparatus, high tension bias generators.

10. (Presently Amended) A method of generating a measure of hard switching amplitude in a switch mode power supply circuit, the circuit including at least one inductive component coupled to an associated switch ~~switching means~~ for cyclically connecting the inductive component to a source of power, the circuit including a signal output representative of a voltage at a junction of the at least one inductive component to the associated switch ~~switching means~~, the method including the steps of:

(a) providing the circuit with a hard switching amplitude detector for deriving the measure of hard switching amplitude occurring in operation in the associated switch ~~switching means~~, the detector including a signal processing path for receiving the signal output and generating the measure of hard switching amplitude therefrom;

(b) imperfectly differentiating the signal output using a signal differentiator circuit ~~differentiating means~~ included in the signal path for generating a corresponding imperfectly differentiated signal; and

(c) integrating the imperfectly differentiated signal in a temporally-gated manner in a signal integration circuit ~~integrating means~~ included in the signal path for generating the measure of hard switching.

11. (New) A switch mode power supply circuit comprising:

a transformer that includes a primary winding electrically isolated from a secondary winding;

a primary switch for cyclically connecting the primary winding to a power source;

a signal output representative of a primary voltage at a junction of the primary winding to the primary switch; and

a hard switching amplitude detector connected at a junction of the secondary winding to a secondary switch, the hard switching amplitude detector including a signal processing path for receiving the signal output and for generating a measure of hard switching amplitude occurring in operation of the primary switch, the signal path including a signal differentiator circuit for imperfectly differentiating the signal output to generate a corresponding imperfectly differentiated signal, a signal integrator circuit for integrating the imperfectly differentiated signal in a temporally-gated manner for generating the measure of hard switching, and a control unit to provide gating signals to the signal differentiator circuit and the signal integrator circuit.

12. (New) The circuit according to claim 11, wherein the control unit is provided with an input signal indicative of a time interval in which hard switching is expected.

13. (New) The circuit according to claim 11, wherein the signal integrator circuit integrates the imperfectly differentiated signal for a period initiated upon detection of a switching peak derived from decay in the primary voltage due to a parasitic capacitance in the primary switch.